IN THE CLAIMS

1-20. (Cancelled).

21. (Previously Presented) A computer system, in which a part of main memory is able to be hot-plugged, said computer system comprising,

a first memory,

a non-volatile storage storing first memory information of said first memory size and a second memory information of a second memory to be hot-plugged,

a processor acquiring said first and second memory information from said non-volatile storage and mapping said first memory based on said first and second memory information, said processor being capable of accessing said non-volatile memory before initialization of an I/O device.

22. (Previously Presented) A computer system according to claim 21,

wherein said processor generating first logical-physical address translating table for said first memory based on said first and second memory information and stores at least a part of said first logical-physical address translating table in said first memory, and

wherein said processor assigns a region to store a second logical-physical address translating table for said second memory in said first memory.

23. (Currently Amended) A computer system according to claim 22,

wherein said first memory has a ~~non-translatable~~ non-address translated region, and

wherein said processor uses said ~~non-translatable~~ non-address translated region for said first and second logical-physical address translating table.

24. (Previously Presented) A computer system according to claim 22,

wherein said processor has TLB.

25. (Previously Presented) A computer system according to claim 21,

wherein said non-volatile storage is EEPROM.

26. (Previously Presented) A computer system comprising,

a first main memory,

a non-volatile storage storing a first configuration information of said first main memory and second configuration information of a second main memory to be hot-added, and

a processor acquiring said first and second configuration information from said non-volatile storage on memory-mapping of said first main memory, said processor being capable of accessing said non-volatile memory before initialization of an I/O device.

27. (Currently Amended) A computer system according to claim 26,

wherein said processor assigns a non-address translated region in said first main memory ~~when~~ <u>on</u> memory-mapping <u>of</u> said first main memory.

28. (Previously Presented) A computer system according to claim 27,

wherein said processor determines size of said non-address translated region based on said first and second configuration information.

29. (Currently Amended) A computer system according to claim 28,

wherein said processor generates a first logical-physical address translation pairs of said first main memory based on said first configuration information and stores at least a part of said <u>first</u> logical-physical address translation pairs in said non-address translated region.

30. (Currently Amended) A computer system according to claim 28,

wherein said processor assigns a region for a second logical-physical address translating pairs of said second main memory in said non-address translated region.

31. (Previously Presented) A computer system according to claim 26,

wherein said non-volatile storage is EEPROM.

32. (Previously Presented) A computer system according to claim 26,

wherein said processor has TLB.

33. (Previously Presented) A computer system, which supports a virtual memory system, said computer system comprising,

a first main memory,

a non-volatile storage storing a first information setting a memory size of a second main memory to be hot-inserted,

a processor mapping said first main memory and acquiring said first information upon said mapping, said processor being capable of accessing said non-volatile memory before initialization of an I/O device.

34. (Currently Amended) A computer system according to claim 33,

wherein said processor ~~assigns~~ includes a top priority region of interrupt handling in said first main memory.

35. (Currently Amended) A computer system according to claim 34,

wherein said processor acquires a memory size of said first main memory and ~~determines~~ assigns said ~~not~~ top priority region ~~from~~ based on said memory size of said first main memory and said first information.

36. (Previously Presented) A computer system according to claim 35,

wherein said processor generates a first logical-physical address translation pairs of said first main memory and stores at least a part of said first logical-physical address translating pairs in said top priority region.

37. (Previously Presented) A computer system according to claim 35,

wherein said processor reserves a region to store a second logical-physical address translation pairs of said second main memory in said top priority region.

38. (Previously Presented) A computer system according to claim 33,

wherein said non-volatile storage EEPROM.

39. (Previously Presented) A computer system according to claim 35,

wherein said processor has a logical-physical address translating unit.

40. (Previously Presented) A computer system according to claim 39,

wherein said processor has TLB.

41. (Previously Presented) A computer system according to claim 21, wherein the non-volatile storage stores the second memory information preliminarily before the second memory is hot-plugged.

42. (Previously Presented) A computer system according to claim 21, wherein the non-volatile storage stores the

second memory information when the computer system is powered on.

43. (Previously Presented) A computer system according to claim 26, wherein the non-volatile storage stores the second configuration information of the second main memory in advance of the hot-adding of the second main memory.

44. (Previously Presented) A computer system according to claim 26, wherein the non-volatile storage stores the second configuration information of the second main memory when the computer system is powered on.

45. (Previously Presented) A computer system according to claim 33, wherein the non-volatile storage stores the first information prior to the hot-insertion of the second main memory.

46. (Previously Presented) A computer system according to claim 33, wherein the non-volatile storage stores the first information when the computer system is powered on.

47. (New) A computer system according to claim 21, wherein said first memory includes a region not subject to address translation and wherein said processor reserves first

and second logical-physical address translating tables in said region not subject to address translation.

48. (New) A computer system according to claim 26, wherein said first memory includes a region not subject to address translation and wherein said processor stores first logical-physical address translating pairs of said first memory in said region not subject to address translation.

49. (New) A computer system according to claim 26, wherein said first memory includes a region not subject to address translation and wherein said processor reserves second logical-physical address translating pairs of said second main memory in said region not subject to address translation.

50. (New) A computer system according to claim 33, wherein said first memory includes a region not subject to address translation and wherein said processor stores first logical-physical address translating pairs of said first main memory in said region not subject to address translation.

51. (New) A computer system according to claim 33, wherein said first memory includes a region not subject to address translation and wherein said processor reserves second

logical-physical address translating pairs of said second main memory in said region not subject to address translation.

52. (New) A computer system according to claim 21, wherein said computer system supports a virtual memory system.

53. (New) A computer system according to claim 26, wherein said computer system supports a virtual memory system.